Rule 1.126 Amd

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~~38~~. A MOSFET according to Claim 35, wherein said gate conducting layer is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.

REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application.

Independent Claim 23 has been amended to more clearly define the present invention over the cited prior art reference by reciting that the source/body contact regions of the MOSFET are laterally spaced apart from the gate conducting layer. A proposed new drawing figure (FIG. 16) is being submitted for the Examiner's convenience to better understand the present invention. No new matter is being added.

In addition, the informality in dependent Claim 24 has been corrected, as helpfully noted by the Examiner. Minor grammatical errors in the specification are being corrected. The specification has also been amended for consistency with the proposed new drawing figure. New Claims 31-38 have been added.

Attached hereto is a marked-up version of the changes made to the claims and to the specification by the current amendment. The attached paper is captioned "Version With Markings to Show Changes Made." The claim amendment and arguments supporting patentability of the claims are presented in detail below.

I. The Claims Are Patentable

The Examiner rejected independent Claim 23 over the

Applicant's prior art FIGS. 1 and 3a-3b. These figures illustrate a conventional trench-gated power MOSFET according to the prior art.

The present invention, as recited in amended independent Claim 23, is directed to a MOSFET comprising a semiconductor layer having a trench therein, a gate dielectric layer lining the trench, and a gate conducting layer in a lower portion of the trench. A dielectric layer is in an upper portion of the trench and extends outwardly from the semiconductor layer. The MOSFET further includes source regions adjacent the outwardly extending dielectric layer, and source/body contact regions laterally spaced apart from the gate conducting layer.

The MOSFET is advantageously formed with a reduced on-resistance without degrading device ruggedness. The on-resistance is reduced since each MOSFET includes a source/body contact region that is laterally spaced apart from the gate conducting layer. The source/body contact region thus provides an efficient short between the source and body regions of the MOSFET. As a result, device ruggedness is increased.

Referring now more particularly to the Applicant's prior art FIGS. 1 and 3a-3b, the Examiner has taken the position that the illustrated MOSFET is the same as the claimed invention. Independent Claim 23 has been amended to recite that the source/body contact regions are laterally spaced apart from the gate conducting layer.

The MOSFET as recited in independent Claim 23 is in sharp contrast to the MOSFET illustrated in FIGS. 1 and 3a-3b.

Reference is directed to page 3, lines 4-15 in the "Background of the Invention" section in the Applicant's specification, which provides:

> "Compared to the conventional trench-gated power MOSFET **10** as shown in FIG. 1, this device **28** provides very high channel densities. The cross sectional views of this device **28** at the different locations labeled 3a and 3b in FIG. 2 are respectively illustrated in FIGS. 3a and 3b. In order to form the device **28** with a very small cell pitch without the stringent requirement of the source/body contact etch mask step, the P+ source/body contact region **18** is interrupted and periodically placed along its N+ stripe, where the N+ source region **26** is completely excluded." (Emphasis added).

The Applicant's prior art FIGS. 1 and 3a-3b illustrate that the source/body contact regions run transverse to the gate conducting layer. In other words, the source/body contact regions in the MOSFET illustrated in FIGS. 1 and 3a-3b are at right angles to the gate conducting layer. In the claimed invention, the source/body contact regions are laterally spaced apart from the gate conducting layer, i.e., they run along side the gate conducting layer. Proposed new drawing FIG. 16 provides a top plan view of the MOSFET to better illustrate that the source/body contact regions are laterally spaced apart from the gate conducting layer.

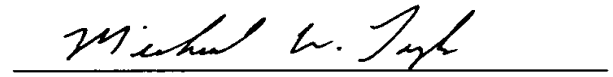
Accordingly, it is submitted that amended independent Claim 23 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b. New independent Claims 31 and 36 are

similar to independent Claim 23. Accordingly, it is submitted that these independent claims are also patentable over the Applicant's prior art FIGS. 1 and 3a-3b. In view of the patentability of the independent claims, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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In re Patent Application of:
ZENG
Serial No. **09/844,347**
Filing Date: **April 27, 2001**
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The following paragraph has been inserted on page 6, between line 31 and page 7, line 1:

FIG. 16 is a top plan view of the trench-gated power MOSFET according to the present invention.

Paragraph beginning at page 9, line 28 has been amended as follows:

A dielectric layer 76 is deposited on the surface of the gate dielectric layer 24 and on the surface of the gate 12. The dielectric layer 76 is for isolating the gate 12. The surface dielectric layer 76 is removed, and the upper surface of the body region 16 and the upper surface of the dielectric layer 20 within the trench 14 [is] are planarized, as illustrated in FIG. 8.

Paragraph beginning at page 10, line 14 has been amended as follows:

Surface portions laterally adjacent the dielectric layer [is] are removed so that a portion of the dielectric layer 20 extends outwardly therefrom, as illustrated in FIG. 9. A thickness of the surface portions that is removed is within a range of about 0.1 to 1 micron. As will be explained in greater detail below, the outwardly extending dielectric

layer 20 advantageously allows self-aligned spacers to be formed.

The following paragraph has been inserted on page 14, between lines 18 and 19:

Referring now to FIG. 16, the top plan view of the trench-gated power MOSFET **70** illustrates that the source/body contact regions are laterally spaced apart from the gate conducting layer **24**. The MOSFET **70** is advantageously formed with a reduced on-resistance without degrading device ruggedness. The on-resistance is reduced since the source/body contact regions **82** are laterally spaced apart from the gate conducting layer **24**. The source/body contact regions **82** thus provide an efficient short between the source and body regions of the MOSFET **70**. As a result, device ruggedness is increased.

In the Claims:

The claims have been amended as follows:

Please cancel Claims 1-22 without prejudice to Applicant's right to file a divisional application directed to the subject matter thereof.

23. (Amended) A MOSFET comprising:
a semiconductor layer having a trench therein;
a gate dielectric layer lining the trench;

a gate conducting layer in a lower portion of the trench;

a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer;

source regions adjacent the outwardly extending dielectric layer; and

source/body contact regions laterally spaced apart from said gate conducting layer.

24. (Amended) A MOSFET according to Claim 23, further [further] comprising a source electrode on said source regions and on said dielectric layer.

New Claims 31 - 38 have been added.

In re Patent Application of:
ZENG
Serial No. **09/844,347**
Filing Date: **April 27, 2001**

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this 19th day of June, 2002.